IN THE CLAIMS

1. (Currently amended) Method for a receiver ~~(1)~~ having a signal path ~~(3)~~ incorporating a tuner ~~(4)~~, a frequency demodulator circuit ~~(5)~~ for supplying an analog stereo multiplex signal comprising a baseband stereo sum signal, a 19 kHz stereo pilot and a stereo difference signal, which is double sideband amplitude-modulated on a suppressed 38 kHz subcarrier, a sampler ~~(6)~~ for converting the analog stereo multiplex signal into a time discrete digital stereo multiplex signal and a stereo decoder ~~(7)~~ for decoding the time discrete digital stereo multiplex signal into a time-discrete digital stereo sum and a time discrete digital stereo difference signal, ~~characterized in that~~wherein the analog stereo multiplex signal is converted into a time discrete digital stereo multiplex signal and then the time discrete digital stereo multiplex signal is shifted over a frequency of 19 kHz to extract at least one of the time-discrete digital stereo sum and the time discrete digital stereo difference signal.

2. (Currently amended) Method as claimed in claim 1, ~~characterized in that~~wherein the 19 kHz shifted signal is further shifted with 19 kHz and then the stereo difference signal is extracted by a low pass filter ~~(12)~~.

3. (Currently amended) Method as claimed in claim 2, ~~characterized in that~~wherein in front of the low pass filter ~~(12)~~ a lower sideband of the stereo difference signal is extracted by a complex filter ~~(11)~~ from the signal shifted twice.

4. (Currently amended) Method as claimed in claim 1, ~~characterized in that~~wherein the

time discrete digital stereo multiplex signal is shifted over a frequency of 19 kHz to extract the time discrete digital stereo difference signal, and wherein the time discrete digital stereo sum signal is extracted from the time discrete digital stereo multiplex signal in a parallel branch ~~(15)~~ by a second low pass filter ~~(16)~~.

5. (Currently amended) Receiver ~~(1)~~ having a signal path ~~(3)~~ incorporating a tuner ~~(4)~~, a frequency demodulator circuit ~~(5)~~ for supplying an analog stereo multiplex signal comprising a baseband stereo sum signal, a 19 kHz stereo pilot and a stereo difference signal, which is double sideband amplitude-modulated on a suppressed 38 kHz subcarrier, a sampler ~~(6)~~ for converting the analog stereo multiplex signal into a time discrete digital stereo multiplex signal and a stereo decoder ~~(7)~~ for decoding the time discrete digital stereo multiplex signal into a time-discrete digital stereo sum and a time discrete digital stereo difference signal, ~~characterized in that~~wherein the stereo decoder ~~(7)~~ comprises two ~~serial~~ frequency shifting circuits ~~(21, 22)~~ connected in series with one another.

6. (Currently amended) Receiver as claimed in claim 5, ~~characterized in that~~wherein the stereo decoder ~~(7)~~ comprises a low pass filter ~~(12)~~ extracting the stereo difference signal.

7. (Currently amended) Receiver as claimed in claim 5, ~~characterized in that~~wherein the stereo decoder ~~(7)~~ comprises a complex filter ~~(11)~~ extracting a lower sideband of the stereo difference signal.

8. (Currently amended) Receiver as claimed in claim 5, ~~characterized in that~~wherein the stereo decoder ~~(7)~~ comprises a second low pass filter ~~(16)~~ extracting the stereo sum signal in a parallel branch ~~(15)~~.

9. (Currently amended) Stereo decoder ~~(7)~~ in a receiver ~~(1)~~ with a frequency demodulator circuit ~~(5)~~, ~~characterized in that~~wherein the stereo decoder ~~(7)~~ comprises two ~~serial~~ frequency shifting circuits ~~(21, 22)~~ connected is series with one another.

10. (Currently amended) Stereo decoder as claimed in claim 9, ~~characterized in that~~wherein the frequency shifting circuits ~~(21, 22)~~ are phase rotators.